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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,877	11/21/2003	Shih Wei Wang	TS02-622	1485

47390 7590 10/19/2005

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,877	WANG ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-10,12-21,23-30 and 32-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10,12-21,23-30 and 32-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed 8 August 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-7,9,21,23-26 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Fastow et al. (U.S. Patent 6,294,430).

Fastow discloses a flash memory device (Figs. 3E and 3G) that contains a substrate (2), source (3) and drain (4) regions, at least a gate stack, disposed over said substrate, situated between said source and drain regions and containing a gate insulator layer (6) over said substrate, a conductive gate layer (70) disposed over said gate insulator layer, with nitrogen atoms (70a) incorporated along the conductive gate layer sidewall and the gate insulator layer-substrate interface.

The semiconductor region (region where source and drain are) is a silicon region, the substrate (2) is a silicon substrate, the gate insulator layer (6) is an oxide layer, the conductive gate layer (70) is a polysilicon layer, the conductive gate layer is a gate of a semiconductor integrated circuit device and the nitrogen atoms (70a) extend to the

conductive gate layer-gate insulator layer interface in the vicinity of the conductive gate layer edge and a sidewall insulator layer made of an oxide

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2,8 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fastow in view of Applicant's Prior Art (Figure 1).

Fastow discloses all the limitations except for a top gate layer disposed on the conductive gate layer and sidewall insulator layer. Whereas Applicant's Prior Art (Fig. 1) contains a semiconductor region within a substrate (2), source and drain regions (4) contained within said semiconductor region, at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer (6) formed over said semiconductor region, a conductive gate layer (8) over said gate insulator layer, a control gate (10) a sidewall insulator layer (16) and a top insulator layer (14) and with disposed over sidewalls of said gate stack. The top insulator is formed to insulate the control gate. (Page 3, lines 1-2) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Fastow by incorporating a top gate stack to insulate the control gate as taught by Applicant's Prior Art (Fig. 1).

Claims 10,12-20,30,32-37 and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Fig. 1) in view of Fastow.

Fastow discloses a flash memory device (Figs. 3e and 3g) that contains a substrate (302), source and drain regions contained within said substrate, at least a gate stack, disposed over said substrate, situated between said source and drain regions and containing a gate insulator layer (304) formed over said substrate, a conductive floating gate layer (308) disposed over said gate insulator layer, an interpoly insulator layer (310) disposed over conductive floating gate, a conductive control gate (312) and a sidewall insulator (314) disposed over sidewalls of gate stacks, with nitrogen atoms (N) incorporated along the conductive floating gate layer sidewall and a sidewall insulator (314). Where the nitrogen atoms are incorporated along the conductive floating gate layer sidewall-sidewall insulator layer interface and the conductive floating gate layer-gate insulator layer interface in the vicinity of the conductive floating gate layer edge and the gate insulator layer-substrate interface.

The substrate (302) is a silicon substrate, the gate insulator layer (304) is an oxide layer, the conductive floating gate layer (308) is a polysilicon layer, the conductive floating gate layer is a gate of a split gate, the interpoly insulator (310) is an ONO layer, sidewall insulator layer (314) is an oxide, the conductive control gate layer (312) is a polysilicon layer

Fastow discloses all the limitations except for a top insulator layer. Whereas Applicant's Prior Art (Fig. 1) contains a split gate transistor (Fig. 1) that contains a substrate (2), source and drain regions (4) contained within substrate, at least a gate

stack, disposed over said substrate, situated between said source and drain regions and containing a gate insulator layer (6) formed over substrate, a conductive floating gate layer (8) over said gate insulator layer, an interpoly insulator layer (12) disposed over said conductive gate layer, a conductive control gate layer (10), a sidewall insulator layer (16) and a oxide top insulator layer (14) disposed over sidewalls of said gate stack and a transfer gate stack comprising a gate insulator, a conductive transfer gate layer that is polysilicon disposed over gate insulator layer that is situated between the gate stack and the source region. The top insulator layer is formed to insulate the control gate and the sidewall insulator layer. (Page 3, lines 1-2) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Fastow by incorporating a top insulator layer to insulate the control gate and the sidewall insulator layer as taught by Applicant's Prior Art.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fastow view of Aminzadeh et al. (U.S. Patent 5,827,769).

Fastow discloses all the limitations except for how the nitrogen treatment is formed. Whereas Aminzadeh discloses a transistor (Figs. 7-8 and 15) that contains a nitride treatment layer (1000) where the treatment is a RTA (rapid thermal processing) or furnace annealing where the RTA process is used with NH3 at a temperature of about 1000 degrees for about 10 seconds. The RTA process is used to increase wafer to wafer uniformity due to the elimination of furnace position variability and to reduce impact on the process thermal budget due to shorter temperature ramp times. (Column 4, lines 32-40) (Column 6, lines 1-15) Therefore it would have been obvious to one

having ordinary skill in the art at the time the invention was made to modify the device of Kurooka by incorporating the RTA process for the nitration treatment to increase wafer to wafer uniformity due to the elimination of furnace position variability and to reduce impact on the process thermal budget due to shorter temperature ramp times as taught by Aminzadeh. Also how the nitrogen treatment is formed is a product by process limitation. A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear. Even though product –by [-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted)."

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fastow and Applicant's Prior Art in view of Aminzadeh et al. (U.S. Patent 5,827,769).

Fastow and Applicant's Prior Art disclose all the limitations except for how the nitrogen treatment is formed. Whereas Aminzadeh discloses a transistor (Figs. 7-8 and 15) that contains a nitride treatment layer (1000) where the treatment is a RTA (rapid thermal processing) or furnace annealing where the RTA process is used with NH3 at a temperature of about 1000 degrees for about 10 seconds. The RTA process is used to increase wafer to wafer uniformity due to the elimination of furnace position variability and to reduce impact on the process thermal budget due to shorter temperature ramp times. (Column 4, lines 32-40) (Column 6, lines 1-15) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Fastow and Applicant's Prior Art by incorporating the RTA process for the nitration treatment to increase wafer to wafer uniformity due to the elimination of furnace position variability and to reduce impact on the process thermal budget due to shorter temperature ramp times as taught by Aminzadeh. Also how the nitrogen treatment is formed is a product by process limitation. A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear. Even though

product –by [-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted)."

Response to Arguments

Applicant's arguments with respect to claims 1,2,4-10,12-21,23-30 and 32-41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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